ABSTRACT OF THE INVENTION

An embedded processor system having a single-chip embedded microprocessor with analog and digital electrical interfaces to external systems. A novel processor core uses pipelined execution of multiple independent or dependent concurrent threads, together with supervisory control for monitoring and controlling the processor thread state and access to other components. The pipeline enables simultaneous execution of multiple threads by selectively avoiding memory or peripheral access conflicts through the types of pipeline stages chosen and the use of dual and tri-port memory techniques. The single processor core executes one or multiple instruction streams on multiple data streams in various combinations under the control of single or multiple threads.